Claims:

1. A method of implementing the compression of a two dimensional bit stream comprising:

receiving the two dimensional bit stream; and

determining whether a predetermined number of bits of the two-dimensional bit stream all have the same binary value.

2. The method of claim 1 further comprising

bypassing a two dimensional compression of the predetermined number of bits if the predetermined number of bits all have the same binary value, otherwise,

compressing a first bit of the predetermined number of bits.

3. The method of claim 2, wherein the two dimensional compression complies with the CCITT Group 4 bi-level image compression standard.

4. The method of claim 1, wherein the two-dimensional bit stream has a run count determined by a plurality of counters.

5. The method of claim 1, wherein the predetermined number of bits is a byte.

6. An integrated circuit comprising:

a logic;

a register; and

the logic and register being coupled so as to implement two dimensional compression of a bit stream by look-ahead of a predetermined number of bits of the bit stream, the predetermined number of bits are a subset of the two dimensional bit stream, and the logic to determine whether the predetermined number of bits all have the same binary value.

7. The integrated circuit of claim 6, wherein the logic is to bypass the two-dimensional compression of the predetermined number of bits if the predetermined number of bits all have the same binary value, otherwise, the logic to compress a first bit of the predetermined number of bits.

8. The integrated circuit of claim 6, wherein said two dimensional compression complies with the CCITT Group 4 bi-level image compression standard.

9. The integrated circuit of claim 6, wherein the logic includes a plurality of counters coupled so that a run count is based at least in part on whether the predetermined number of bits all have the same binary value.

10. The integrated circuit of claim 6, wherein the logic is coupled to detect a change in a state of the bit stream.

11. The integrated circuit of claim 6, wherein the predetermined number of bits is eight.

12. A document processing system comprising:

a logic and a register, the logic and the register being coupled so as to implement two dimensional compression of a bit stream by look-ahead of a predetermined number of bits of the bit stream, the predetermined number of bits are a subset of the two dimensional bit stream, and the logic to bypass compression of the predetermined number of bits if the predetermined number of bits all have the same binary value.

13. The document processing system of claim 12, wherein said two-dimensional compression to be implemented complies with the CCITT Group 4 bi-level compression standard.

14. The document processing system of claim 12, wherein the logic includes a first and second binary counter, the first and second binary counter being coupled so as to calculate a run count based at least in part on whether the predetermined number of bits all have the same binary value.

15. The document processing system of claim 12, wherein the logic is to perform two-dimensional compression of a first bit of the predetermined number of bits, if the predetermined number of bits do not have the same binary value.